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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/985,766	11/06/2001	Hiroyuki Utsumi	1448.1017	4337

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EXAMINER	
CHEN, TSE W	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 09/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/985,766	UTSUMI ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5172004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on May 17, 2004 was filed before the mailing date of the first Office Action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bock et al., U.S. Patent 5155856, hereinafter Bock, in view of IBM Technical Disclosure Bulletin ACC-NO NN79013353, hereinafter IBM, and MacGinitie et al., U.S. Patent 4688212, hereinafter MacGinitie.

4. In re claim 1, Bock discloses a processor [processing unit 1] comprising:

- A first initial setting area [S area] which is initialized based on an input of a first reset signal [power on reset POR] [fig.2-4; col.3, ll.21-31; col.4, ll.26-39].
- A second initial setting area [I area] which is initialized based on an input of either the first reset signal or a second reset signal [system reset normal SRN] [fig.2-4; col.3, ll.32-46; col.4, ll.26-39].

- Wherein when either one of the first and second reset signals is input, initial setting area/s correspondingly is/are initialized out of the first and second initial setting areas [fig.2; col.3, ll.32-48].

5. Bock did not discuss the non-overlapping of the initial setting areas or explicitly address the issue of preventing access to the selected areas during initialization of the areas.

6. In regards to the non-overlapping of the initial setting areas, IBM discloses a processor [microprocessor] comprising:

- Initial setting areas [functional areas] which are initialized based on an input of a reset signal [reset line] and which do not overlap with each other [functional areas associated with predefined addresses do not overlap].

7. It would have been obvious to one of ordinary skill in the art, having the teachings of Bock and IBM before him at the time the invention was made, to modify the processor taught by Bock to include the non-overlapping configuration taught by IBM, in order to obtain the processor with a first initial setting area which is initialized based on an input of a first reset signal, a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal and which do not overlap with said first initial setting area. The non-overlapping configuration taught by IBM is a very well known configuration suitable for use with the processor of Bock. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reset non-overlapping areas [IBM].

8. In regards to the issue of preventing access to the selected areas during initialization of the areas, MacGinitie discloses a processor [TTIS] comprising:

- A flag [EFQ bit] that is cleared [0] by an input of a reset signal [power up reset] and that is set [1] when initial setting of an initial setting area [Q size register] has been completed [col.13, ll.20-22].
- Wherein initial setting area corresponding to the cleared flag [col.13, ll.20-22; register is initialized which corresponds to the flag that is set].

9. It would have been obvious to one of ordinary skill in the art, having the teachings of Bock and MacGinitie before him at the time the invention was made, to modify the processor taught by Bock to include the flag indicator taught by MacGinite, in order to obtain the processor with the limitations taught by Bock, that further comprises:

- A first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed.
- A second flag that is cleared by an input of either the first or second reset signals and that is set when initial setting of the second initial setting area has been completed [MacGinitie: col.13, ll.23-30; one with ordinary skill in the art would recognize that another flag still must be set to prevent access to second initial setting area during initialization according to MacGinitie teaching].
- Wherein when either one of the first and second reset signals is input, initial setting area/s corresponding to cleared flag/s is/are initialized out of the first and second initial setting areas.

10. The flag indicator taught by MacGinitie is a very well known indicator suitable for use with the processor of Bock. One of ordinary skill in the art would have been motivated to make

such a combination as it provides a way to prevent access to an area being initialized [col.13, ll.20-30].

11. As to claim 2, Bock, IBM, and MacGinitie disclose each and every limitation of the claim as discussed above in reference to claim 1. In particular, Bock discloses the processor that further comprises:

- A third initial setting area [F area] which is initialized based on an input of the first or second reset signals or a third input signal [check reset CHR] [fig.2-4; col.3, ll.32-48; col.4, ll.26-39].

12. As to claim 3, Bock discloses the processor wherein:

- The first initial setting area [S area] is formed by a first register group [shift register latches SRL] for performing communication between the processor and an outside of the processor [fig.1; col.1, ll.42-54; col.2, ll.10-36, ll.55-57; S area contains the shift register latches representing internal processing state of communication].
- The third initial setting area [F area] is formed by a second register group relating to execution of instructions [microprogram] inside the processor [col.3, ll.5-9].

13. IBM further discloses the processor wherein:

- A second initial setting area is an area other than both a first register group and a second register group [areas don't overlap].

14. As to claim 4, Bock, IBM, and MacGinitie disclose each and every limitation of the claim as discussed above in reference to claim 1. In particular, Bock discloses n-th instances of the limitations [col.2, ll.37-53].

15. As to claim 5, Bock discloses that the processor is provided with an external input terminal [main switch] for receiving the respective reset signals from the outside [user] [col.1, ll.31-35; col.2, l.67 – col.3, l.4].

16. As to claim 6, Bock discloses the processor wherein the respective reset signals are generated within the processor [col.1, ll.18-24; col.3, ll.5-20; error or failure causes reset].

17. As to claim 7, Bock, IBM, and MacGinitie disclose each and every limitation of the claim as discussed above in reference to claim 1. As set forth, Bock, IBM, and MacGinitie teaches the processor; therefore, Bock, IBM, and MacGinitie teaches the method of controlling resetting of the processor. Futhermore, MacGinitie and Bock discloses the method comprising:

- The step in which the flag [bit] that correspond to a reset signal type is cleared [MacGinitie: col.13, ll.20-22].
- The step in which a state of the flag is confirmed [MacGinitie: col.13, ll.23-30; operates according to confirmation of flag state], initial setting [0] is performed for an initial setting area corresponding to the cleared flag and, after the initial setting is completed, setting corresponding flags is repeatedly performed until all of the flags are placed in a set state [1] [col.13, ll.20-22; one with ordinary skill in the art would recognize that the single flag instance would have to be extended to multiple flags in order to prevent access and abnormal function for Bock].

18. As to claim 8, Bock, IBM, and MacGinitie disclose each and every limitation of the claim as discussed above in reference to claim 1. As set forth, Bock, IBM, and MacGinitie teaches the processor; therefore, Bock, IBM, and MacGinitie teaches the method of controlling resetting of the processor. Futhermore, MacGinitie and Bock disclose the method comprising the steps of:

- Clearing the first flag if the first reset signal is received, and clearing the first and second flags if the second reset signal is received [MacGinities: col.13, ll.20-22; since the second reset signal clears both first and second areas for Bock, one with ordinary skill in the art would recognize that the single flag instance would have to be extended to multiple flags in order to prevent access and abnormal function for Bock].
- Checking which flag/s has/have been cleared out of the first and second flags [MacGinitie: col.13, ll.23-30; operates according to confirmation of flag state].
- Initializing [0] initial setting area/s corresponding to the cleared flag/s out of the first and second areas and setting flag/s [1] corresponding to the initial setting area/s which has/have been initialized out of the first and second areas [col.13, ll.20-22; one with ordinary skill in the art would recognize that the single flag instance would have to be extended to multiple flags in order to prevent access and abnormal function for Bock].

19. As to claim 9, Bock, IBM, and MacGinitie disclose each and every limitation of the claim as discussed above in reference to claims 1, 2, and 8. As set forth, Bock, IBM, and MacGinitie teaches the processor; therefore, Bock, IBM, and MacGinitie teaches the method of controlling resetting of the processor.

20. As to claim 10, Bock, IBM, and MacGinitie disclose each and every limitation of the claim as discussed above in reference to claims 3 and 9.

21. As to claim 11, Bock, IBM, and MacGinitie disclose each and every limitation of the claim as discussed above in reference to claims 1, 2, 4, and 8. As set forth, Bock, IBM, and MacGinitie teaches the processor; therefore, Bock, IBM, and MacGinitie teaches the method of controlling resetting of the processor.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additionally cited U.S. patent documents describes various methods for resetting non-overlapping areas and checking associated flags for resetting.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
August 31, 2004

REHANA PERVEEN
PRIMARY EXAMINER